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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/792,141	03/02/2004	Matthew L. Bibee	X-1537 US	4860

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EXAMINER	
SEMENENKO, YURIY	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/792,141	BIBEE, MATTHEW L.	
	Examiner	Art Unit	
	Yuriy Semenenko	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10 and 12-29* is/are pending in the application.

4a) Of the above claim(s) *12-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10 and 27-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Amendment filed on 06/22/2006 has been entered. In response to the Office Action dated 03/30/2006, Applicants have amended claims 1, 3, 5 and 9. Claims 2 and 11 has been cancelled. Claims 27-29 are newly added. Claims 1 and 3-10 and 12-29 are now pending in the application.

Response to Arguments

2.1. Applicant's arguments filed 2/06/2006 have been considered but are moot in view of the new grounds of rejection. Nevertheless, Examiner points out, in response to Applicant's arguments with respect to independent claim 7 Payne's, Patriche's and Goergen's references in combination teach all of the limitations of the claim 7. As clearly shown in Fig. 14 there are two rows of the ground vias between the pair of the rows of the signal vias which is exactly as claimed in claim 7.

Claim Objections

3.1. Claims 13-16 are objected to because of the following informalities: Claims 13-16 should be amended to change "The printed circuit board " to "The printed circuit board assembly" as dependent from claim 12, which claimed " A printed circuit board assembly".

Appropriate correction is required.

3.2. Claim 8 are objected to because of the following informalities: unclear term "vias...open". Should change limitation "vias....open" , because there is not such term mentioned anywhere in the Specification.

Specification

4. The disclosure is objected to because of the following informalities:

Page 4: Wrong name of the section. It should be - DETAILED DESCRIPTION OF THE INVENTION-

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5.1. Claims 1, 3, 4 and 6 are rejected under 35U.S.C. 103(a) as being unpatentable over Payne (PGPub #2004/0264153) hereinafter Payne in view of Patriche (Patent # 6608762) hereinafter Patriche.

As to claim 1: Payne discloses in Fig. 14 a printed circuit board 50 having signal vias 52a and ground vias 53a, said printed circuit board comprising: a first row of vias 52a having a plurality of signal vias (first row of signal vias from left side of the Fig. 1); a second row of vias 52a having a plurality of signal vias (second row of signal vias from left side of the Fig. 1), said second row of vias being consecutive with said first row of vias; and a plurality of rows of vias 53a between said first row of vias and said second row of vias, said plurality of rows of vias being coupled to a ground plane (column 5, lines [0065]),

except, Payne does not explicitly teach vias of at least one row of said plurality of rows of vias are adapted to receive leads of a component attached to said printed circuit board.

Patriche discloses in Fig. 4 vias 54 of at least one row of said plurality of rows of vias, Fig. 3, are adapted to receive leads of a component 40, fig. 4 attached to said printed circuit board 16 (column 5, lines 14-19).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Payne to include in his invention that vias of at least one row of said plurality of rows of vias are adapted to receive leads of a component attached to said printed circuit board to improve signal propagation performance as taught by Patriche (column 1, lines 59-62).

As to claim 3: Payne, as modified, discloses in Fig. 14 the printed circuit board of claim 1 wherein said plurality of rows of vias comprises at least one row of vias 53a adjacent said first row of vias 52a.

As to claim 4: Payne, as modified, discloses in Fig. 14 the printed circuit board of claim 3 wherein said plurality of rows of vias comprises at least one row of vias 53a adjacent said second row of vias 52a.

As to claim 6: Payne, as modified, discloses in Fig. 14 the printed circuit board of claim 3 wherein said plurality of rows of vias 53a between said first row of vias 52a and said second row of vias 52a comprises a row of vias receiving a ground lead 254a of a component 250.

5.2. Claims 7, 8 and 27-29 are rejected under 35U.S.C. 103(a) as being unpatentable over Payne in view of Patriche and in view of Goergen (Patent # 6822876) hereinafter Goergen.

As to claim 7: Payne discloses in Fig. 14 a printed circuit board 50 having signal vias 52a and ground vias 53a, said printed circuit board comprising: rows of vias having signal vias 52a, said signal vias receiving leads 240 of a component 200, Fig. 12b; a rows of vias having ground vias between said rows of vias having signal vias; and a row of vias having ground vias 53a between the rows of vias having ground vias, said ground vias 53a receiving other leads 250 of said component 200,

except, Payne does not explicitly teach a pair of rows of vias.

Goergen discloses in Fig. 4 a differential pair of rows of vias 102, 104, 106, 108 (column 7, lines 1-2).And further this differential pair remains aligned with a row of ground thru-holes 120a, 120b, Fig. 5.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Payne to include in his invention a pair of rows of vias to produce a reliable communication pair differential-signaling speed up 10.7 Gbps backplane, as taught by Goergen.

As to claim 8: Examiner interprets the language claims 8 and 11 "pair of rows of vias having ground vias remains open" to mean that the ground via has a pad for connecting to component not merely directly connecting pin of component to via.
Payne, as modified, discloses the printed circuit board, having all of the claimed features as discussed above with respect claim 7 wherein the rows of vias having

ground vias 53a, Fig. 14 remains open. Ground conductor is connecting to conductive via 53a by mounting pad 53 (page 5, [0062]),

except, Payne does not explicitly teach a pair of rows of vias.

Goergen discloses in Fig. 4 a differential pair of rows of vias 102, 104, 106, 108 (column 7, lines 1-2).And further this differential pair remains aligned with a row of ground thru-holes 120a, 120b, Fig. 5.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Payne to include in his invention a pair of rows of vias to produce a reliable communication pair differential-signaling speed up 10.7 Gbps backplane, as taught by Goergen.

As to claims 27-29: Payne, as modified, discloses the printed circuit board, having all of the claimed features as discussed above with respect claim 7, wherein said vias of said pair of rows of vias having ground vias 83, Fig. 16,are aligned with vias of said pair of rows of vias having signal vias 82 (page 5, [0068]).
Allthough, Payne does not explicitly teach a first row of vias of said pair of rows of vias having signal vias comprises vias of a first set of differential pairs of signal vias; and a second row of vias of said pair of rows of vias having signal vias comprises vias of a second set of differential pairs of signal vias, at time the invention was made, it was old and well-know to use different patterns of the laid out of the differential pairs of the signal vias, as evidenced by Goergen (column 7, lines 33-39).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Payne to include in his invention a first row of vias of said pair of rows of vias having signal vias comprises vias of a first set of differential pairs of signal vias; and a second row of vias of said pair of rows of vias having signal vias comprises vias of a second set of differential pairs of signal vias to produce a reliable communication pair differential-signaling speed up 10.7 Gbps backplane, as taught by Goergen (column 2, lines 1-7).

5.3. Claims 5, 9 and 10 are rejected under 35U.S.C. 103(a) as being unpatentable over Payne in view of Patriche and in view of Goergen and in view of Cartier et al. (Patent # 6639154) hereinafter Cartier.

As to claims 5 and 9: Payne, as modified, discloses the printed circuit board, having all of the claimed features as discussed above with respect claim 4 (7), wherein at least one of vias receiving leads of a component,

except, Payne does not explicitly teach one row of said plurality of rows of vias comprises vias having a smaller diameter than vias of said at least one row of said plurality of rows of vias adapted to receive leads of a component.

Cartier discloses in Fig. 2 and 3 the rows of vias 48 adjacent said first row of vias 46 and said second row of vias comprise vias having a smaller diameter than vias 48 of the at least one of vias 50.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Payne to include in his invention that one row of said plurality of rows of vias comprises vias having a smaller diameter than vias of said at least one row of said plurality of rows of vias adapted to receive leads of a component, as taught by Cartier because Cartier teaches that such configuration provide positioning of the ground vias closer to the signal via (column 6, lines 63-67 and lines 7, lines 1-7).

As to claim 10: Payne, as modified, discloses the printed circuit board, having all of the claimed features as discussed above with respect claim 7,

except, Payne does not explicitly teach said [pair] of rows of vias having ground vias provides return current paths for signals in said signal vias.

Cartier discloses rows of vias having ground vias provides return current paths for signals in said signal vias (column 7, lines 43-47).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Payne to include in his invention rows of vias having ground vias provides return current paths for signals in said signal vias, as taught by Cartier

because Cartier teaches that such configuration provide superior electrical contact with connector (column 7, lines 45-47).

Payne also fail to disclose that row is a pair of rows of vias.

Goergen discloses in Fig. 4 a differential pair of rows of vias 102, 104, 106, 108 (column 7, lines 1-2). And further this differential pair remains aligned with a row of ground thru-holes 120a, 120b, Fig. 5.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Payne to include in his invention a pair of rows of vias to produce a reliable communication pair differential-signaling speed up 10.7 Gbps backplane, as taught by Goergen.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7.1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

7.2. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571)- 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7.3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YS

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